REMARKS

In sections 2-4 of the final Office Action, the Examiner rejects claims 2 and 38 under 35 USC 112, second paragraph, asserting that the limitation "a capacitor coupled between the pad and the first doped region" in claims 2 and 38 is in conflict with the phrase "electrically floated in independent claims 1 and 34. The Applicants respectfully disagree and have discussed this issue in the last response and in the telephone interviews with the Examiner and the Examiner's supervisor. The Applicants maintain their position. However, rather than belabor this point further, the Applicants have rewritten claims 2 and 38 into independent form. Claim 2 now includes all limitations of claim 1 (allowed) except the phrase "electrically floated in the well region". Thus, claim 2 should now be allowable. Claim 38 now includes all limitations of original claim 34 except the phrase "electrically floated in the well region". Since the phrase "electrically floated" and the limitation of the capacitor do not appear at the same time, the Applicants believe that the rejection under 35 USC 112, second paragraph has been overcome.

In the Advisory Action, the Examiner asserts that since a capacitor is a source of voltage, a doped region cannot be electrically floated in a well and at the same time be connected to a capacitor. Note that a capacitor is a source of AC voltage, not a source of DC voltage. The term "electrically floated" only refers to DC condition but not AC condition.

In sections 5-6 of the final Office Action, the Examiner rejects claims 34-35 and 37 under 35 USC 102(b) as being anticipated by Ham (US Patent No. 5,903,420). The Applicants respectfully traverse this rejection and have discussed this issue in the last response and in the telephone interviews with the Examiner and the Examiner's supervisor. In particular, the Applicants believe that since the doped region 46 in Ham is coupled to V_{SS} through the P-well 22 or coupled to the V_{DD} through the N-well 24 (see e.g. Figs. 6-7 and col. 4, lines 17-20), the doped region 46 has DC paths coupled to V_{SS} or V_{DD} and is, by definition, not "electrically floated", as recited by claim 34. Thus, the Applicants believe that the original claim 34 is patentable over Ham. However, in order to save time and expenses, the Applicants have amended claim 34 so that it now recites, in part, "a third doped region of the first conductive type disposed in the well region, and electrically floated in the well region so that the third doped region has no DC connection to the first node, wherein the first node is electrically coupled to the first doped region and the well region, and the second node is electrically coupled to the second doped region."

As shown in Fig. 6 of Ham, the region 46 is coupled to the V_{DD} through the region 52 and the N-well if the region 46 is N type. Also, the region 46 is coupled to the V_{SS} through the region 40 and the P-well if the region 46 is P type. Thus, the region 46 is electrically coupled to V_{SS} or V_{DD} through the regions 40 or 52 when the region 46 is P-type or N-type. Since region 46 has DC connections, it is not a third doped region "electrically floated in the well region so that the third doped region has no DC connection to the first node", as recited by claim 34 of the present application. Thus, the Applicants believe that claim 34 is patentable. Claims 35 and 37 are also patentable, at least by virtue of their dependency from claim 34.

New claim 39 recites, in part, "wherein the first doped region is ... electrically floated in the well in that there is no DC connection between the first doped region and the pad". Claim 39 is patentable for the same reasons as claim 34.

The Applicants believe that all pending claims are now in condition for allowance. Reconsideration of this application is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

Enclosed please find a copy of Troy Guangyu Cai's Notice of Limited Recognition under 35 CFR 10.9(b) to prepare and prosecute patent applications wherein the patent applicant is a client of Ladas & Parry, and the attorney of record in the applications is a registered practitioner who is a member of Ladas & Parry.

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May 29, 2003
(Date of Deposit)

Troy Guangyu Cai
(Name of Applicant, Assignee or Registered Representative)


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Appendix A

Marked-up Copy of the Amended Claims

2. (Amended) [The output buffer of claim 1, wherein the second circuit further comprises] An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, comprising:

a resistor constructed by a well region of a second conductivity type deposited on a substrate of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region of the second conductivity type at least partially overlapping the well region and coupled to the pad;

a first doped region of the first conductivity type, deposited in the well region;

a capacitor coupled between the pad and the first doped region; and

an electrostatic discharge protection component, coupled between the second end and the second power line.

34. (Amended) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductive type;

a first doped region and a second doped region of a second conductive type formed in the substrate, the first and second doped regions being spaced apart enabling a channel region formed in between;

a well region of the second conductive type, formed in the substrate; and

a third doped region of the first conductive type[, electrically floated] disposed in the well region, and electrically floated in the well region so that the third doped region has no DC connection to the first node, wherein the first node is electrically coupled to the first doped region and the well region, and the second node is electrically coupled to the second doped region.

38. (Amended) [The electrostatic discharge protection circuit as claimed in claim 34,] An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductive type;

a first doped region and a second doped region of a second conductive type formed in the substrate, the first and second doped regions being spaced apart enabling a channel region formed

in between;

a well region of the second conductive type, formed in the substrate; and

a third doped region of the first conductive type disposed in the well region,

wherein the third doped region is coupled to the first node through a capacitor,

wherein the first node is electrically coupled to the first doped region and the well region, and the second node is electrically coupled to the second doped region.